REMARKS

This application has been carefully reviewed in light of the Office Action dated March 29, 2004. Claims 1, 2, 5 and 6 remain pending in the application, with Claim 7 having been cancelled herein. Claims 1 and 6 are the independent claims. Reconsideration and further examination are respectfully requested.

Applicants are submitting herewith a Replacement Sheet for Figure 1, which has been amended to correct an error noted in that figure. More specifically, the sub-scanning direction has been amended to correctly identify that direction as being perpendicular to the main-scanning direction along the end facet of the chip that has the luminous spots. Additionally, the sub-scanning direction as originally denoted on Figure 1 has been corrected to reflect that it is actually the resonator length direction as described in the specification. No new matter has been added and Applicants respectfully request approval of the changes incorporated in the Replacement Sheet.

Claims 1, 2 and 5 were rejected under 35 U.S.C. § 103(a) over Japan 61-206286 (Kazuo) in view of U.S. Patent 6,034,982 (Iwase), and Claims 6 and 7 were rejected over Japan 10-48557 (Nakanishi) in view of Kazuo and Iwase. These rejections are respectfully traversed and the Examiner is requested to reconsider and withdraw the rejections in light of the following comments.

The present invention concerns maintaining polarization angles between lasers in semiconductor laser arrays. According to the invention, a chip having a plurality of luminous spots is soldered to a mount in a junction down fashion. When the chip is soldered, an end facet of the chip having the plurality of luminous spots is arranged so that

it projects from a corresponding end facet of the mount in a resonator length direction. The amount of projection is set such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount. For example, as seen in Figure 1, when the chip is soldered to the mount, the end facet of the chip projects by an amount T (which may be tens of several micrometers) from the corresponding end facet of the mount. Thus, the luminous spots are further away from the soldered area, thereby reducing the residual stress near the luminous spots. As a result, the polarization angle difference between the luminous spots is reduced.

With specific reference to the claims, amended independent Claim 1 is a semiconductor laser array comprising a chip having a plurality of luminous spots, the chip having buried heterojunction type lasers, and a mount for mounting the chip by means of solder, the chip being soldered to the mount in a fashion of junction down, wherein the chip projects from a corresponding end facet of the mount with a side of the chip having the plurality of luminous spots projecting away from the corresponding end facet of the mount, and wherein the chip has a length between 200 μm and 300 μm in a resonator length direction and projects from the corresponding end facet of the mount in the resonator length direction by a predetermined amount such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount.

Amended independent Claim 6 is an optical scanner claim that includes

features substantially corresponding to those of Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1 and 6, and in particular is not seen to disclose or to suggest at least the feature of a chip, having heterojunction type lasers, being soldered to the mount, in a fashion of junction down, wherein the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of the mount in a resonator length direction by a predetermined amount such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount.

Kazuo is merely seen to disclose bonding a laser chip 9 onto a semiconductor wafer 1 such that a laser beam emitting end facet 11 projects slightly into a groove 8 of the wafer 1. Thus, while the chip of Kazuo may project slightly beyond a surface of the groove, the reason for the slight projection is believed to be based on reducing reflection of emitted laser beams on the top surface of the substrate 1. Additionally, Applicants have found nothing in Kazuo that indicates that the amount of projection is based on a predetermined amount such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount. Accordingly, Kazuo is not seen to disclose or to suggest the foregoing features of Claims 1 and 6.

Nakanishi and Iwase have been studied but are not seen to add anything

that, when combined with one another or with Kazuo, would have disclosed or suggested the features of the present invention. More particularly, Nakanishi is merely seen to disclose deflecting laser light by a rotating polygon mirror so that an image is formed on a photoreceptor through a plastic lens. However, Nakanishi, like Kazuo, is not seen to disclose or to suggest at least the feature of a chip, having heterojunction type lasers, being soldered to the mount, in a fashion of junction down, wherein the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of the mount in a resonator length direction by a predetermined amount such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount.

Iwase is merely seen to disclose a semiconductor laser array mounted to a sub-mount by soldering the array flush with the end facet of the sub-mount. Accordingly, Iwase is also not seen to disclose or to suggest at least the feature of a chip, having heterojunction type lasers, being soldered to the mount, in a fashion of junction down, wherein the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of the mount in a resonator length direction by a predetermined amount such that residual stresses near each of the plurality of luminous spots caused by the soldering are reduced so as to maintain an angle of polarization between the plurality of luminous spots within a predetermined amount.

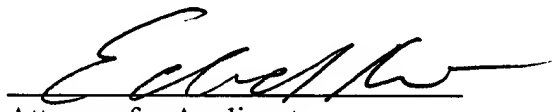
In view if the foregoing deficiencies of the applied art, in which none of the

references alone or in any permissible combination are seen to disclose the features of the present invention, amended independent Claims 1 and 6, as well as the claims dependent therefrom, are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California, office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,



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